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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
09/321,605	05/28/99	SASHIDA	N 990535

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EXAMINER	
CHEN, I	
ART UNIT	PAPER NUMBER
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Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

Office Action Summary	Application No. 09/321,605	Applicant(s) Sashida et al.
	Examiner Jack Chen	Art Unit 2813

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) ☒ Responsive to communication(s) filed on *Jun 25, 2001* .

2a) ☒ This action is **FINAL.** 2b) ☐ This action is non-final.

3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

Disposition of Claims

4) ☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above, claim(s) *17-20* is/are withdrawn from consideration.

5) ☐ Claim(s) _____ is/are allowed.

6) ☒ Claim(s) *1-16, 21, and 22* is/are rejected.

7) ☐ Claim(s) _____ is/are objected to.

8) ☐ Claims _____ are subject to restriction and/or election requirement.

Application Papers

9) ☐ The specification is objected to by the Examiner.

10) ☐ The drawing(s) filed on _____ is/are objected to by the Examiner.

11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved.

12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

13) ☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

a) ☐ All b) ☐ Some* c) ☐ None of:

1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

*See the attached detailed Office action for a list of the certified copies not received.

14) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

Attachment(s)

15) ☐ Notice of References Cited (PTO-892)

16) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

17) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s). 5

18) ☐ Interview Summary (PTO-413) Paper No(s). _____

19) ☐ Notice of Informal Patent Application (PTO-152)

20) ☐ Other:

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-16, 21-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mochizuki et al., U.S./5,990,507 in view of Ochiai, U.S./5,943,583 or Watanabe et al., U.S./5,481,490 or Zafar, U.S./5,750,419.

Mochizuki et al. discloses a method of forming a semiconductor device, which comprises forming an impurity diffusion layer S/D in a substrate; forming a first insulating film 9/10/13/16/51/121/122 covering the substrate; forming a lower electrode 17/17a of a capacitor on the first insulating film; forming an oxide dielectric film 18 of the capacitor on the lower electrode; forming an upper electrode 19 of the capacitor on the oxide dielectric film; forming a second insulating film 20/13/52 for covering the capacitor; forming a first opening for electrically connecting the impurity diffusion layer and a second opening on the upper electrode in the first and second insulating films, by etching a part of the second insulating film and a part of the first insulating film (figs. 12, 17, 19, 20, 21, 22, 23); forming a metal 21/22/11'/36/111 (titanium nitride, figs. 12, 17, 19, 20, 21, 22, 23) film on the second insulating film for connecting

electrically the impurity diffusion layer via the first opening and the upper electrode via the second opening; forming a local interconnection in a range which pass through the first opening and the second opening and contains at least a region where the upper electrode contacts the oxide dielectric film (see figs. 12, 17, 19, 20, 21, 22, 23; layer 21/22/11'/111, which shows the local interconnection in a range which pass through the first opening and the second opening, and contains at least a region where the upper electrode contacts the oxide dielectric film, 18 contacts with 19), by patterning the metal film, or forming a local interconnection covering an entire portion of the upper electrode with an area which is larger than an area where the upper electrode contacts with the oxide dielectric film in a plan view (i.e., at a plane parallel to the drawing figures, i.e., see figs.17, 19, 20, 21, 22, 23), in a range which passes through the first opening and the second opening, by patterning the metal film 22/11' fig. 17, also see fig. 19, layers 22/11' or 36/11' or fig. 20, layer 22, or fig. 21, layers 111/22/11' or fig. 22, layers 22/11' or fig. 23, layers 11/22); wherein the local interconnection is a blocking layer for preventing a diffusion of a redundant to the oxide dielectric film (since the same material (TiN) is used for the metal layer, which is the same as applicant's claimed invention); and forming a third insulating film 23/30 for covering the local interconnection, see figs. 1-28, cols. 1-40.

However, Mochizuki et al. does not explicitly shows forming a first opening which exposes the impurity diffusion layer.

It is well known in the art to forming the first opening which exposes the impurity diffusion layer, such will allow the formation of the self-align contacts and eliminate the

misalignment of the contact and simplify the processing steps. For example, Ochiai discloses a method of forming a semiconductor device, which comprises forming an impurity diffusion layer 8 in a substrate 4; forming a first insulating film 62 covering the substrate; forming a lower electrode 31 of a capacitor on the first insulating film; forming an oxide dielectric film 2 of the capacitor on the lower electrode; forming an upper electrode 32 of the capacitor on the oxide dielectric film; forming a second insulating film 63 for covering the capacitor; forming a first opening which expose the impurity diffusion layer and a second opening which exposes the upper electrode in the first and second insulating films, by etching a part of the second insulating film and a part of the first insulating film; forming an metal film 11 on the second insulating film for connecting electrically the impurity diffusion layer via the first opening and the upper electrode via the second opening; forming a local interconnection in a range which pass through the first opening and the second opening and contains at least a region where the upper electrode contacts the oxide dielectric film (fig. 4), by patterning the metal film, see figs. 1-5, cols. 1-8. Watanabe et al. also discloses the similar processes as above, see figs. 1-9, cols. 1-16.

Zafar also discloses a method of forming a semiconductor device, which comprises forming an impurity diffusion layer 204 in a substrate 20; forming a first insulating film covering the substrate; forming a lower electrode of a capacitor on the first insulating film; forming an oxide dielectric film 244 of the capacitor on the lower electrode; forming an upper electrode 246 of the capacitor on the oxide dielectric film; forming a second insulating film 32 for covering the capacitor; forming a first opening which exposes the impurity diffusion layer and a second

opening which the upper electrode in the first and second insulating films, by etching a part of the second insulating film and a part of the first insulating film (fig. 3); forming an metal film on the second insulating film for connecting electrically the impurity diffusion layer via the first opening and the upper electrode via the second opening; forming a local interconnection in a range which pass through the first opening and the second opening and contains at least a region where the upper electrode contacts the oxide dielectric film (figs. 4-5), by patterning the metal film; and forming a third insulating film 522/524 for covering the local interconnection such will eliminate the short circuit problems, see figs. 1-6, cols. 1-8.

Therefore, the subject matter as a whole would have been obvious to one having ordinary skill in the art at the time the invention was made to further modify the standard process of Mochizuki et al. with the teaching of Ochiai or Watanabe et al. or Zafar because of the desirability to improve the performance of the device (i.e., eliminate misalignments of the contacts/plugs, and simplify the processing steps such will decrease the cost).

3. Claims 1-13, 16, 21-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ochiai, U.S./5,943,583 or Watanabe et al., U.S./5,481,490 taken with Zafar, U.S./5,750,419 and in view of Kawai et al., U.S./6,022,774 and Yamazaki et al., U.S./6,046,469.

Ochiai discloses a method of forming a semiconductor device, which comprises forming an impurity diffusion layer 8 in a substrate 4; forming a first insulating film 62 covering the substrate; forming a lower electrode 31 of a capacitor on the first insulating film; forming an oxide dielectric film 2 of the capacitor on the lower electrode; forming an upper electrode 32 of the

capacitor on the oxide dielectric film; forming a second insulating film 63 for covering the capacitor; forming a first opening which exposes the impurity diffusion layer and a second opening which exposes the upper electrode in the first and second insulating films, by etching a part of the second insulating film and a part of the first insulating film; forming an metal film 11 on the second insulating film for connecting electrically the impurity diffusion layer via the first opening and the upper electrode via the second opening; forming a local interconnection in a range which pass through the first opening and the second opening and contains at least a region where the upper electrode contacts the oxide dielectric film (fig. 4), by patterning the metal film, wherein the local interconnection is a blocking layer for preventing a diffusion of a redundant to the oxide dielectric film; see figs. 1-5, cols. 1-8. Watanabe et al. also discloses the similar processes as above, see figs. 1-9, cols. 1-16.

However, the above references do not expressively show forming a local interconnection covering an entire portion of the upper electrode; and forming a third insulating film for covering the local interconnection, and using titanium nitride as the metal film (11) and carrying out various steps of oxygen annealing.

Zafar discloses a method of forming a semiconductor device, which comprises forming an impurity diffusion layer 204 in a substrate 20; forming a first insulating film covering the substrate; forming a lower electrode of a capacitor on the first insulating film; forming an oxide dielectric film 244 of the capacitor on the lower electrode; forming an upper electrode 246 of the capacitor on the oxide dielectric film; forming a second insulating film 32 for covering the capacitor;

forming a first opening which exposes the impurity diffusion layer and a second opening which exposes the upper electrode in the first and second insulating films, by etching a part of the second insulating film and a part of the first insulating film (fig. 3); forming an metal film on the second insulating film for connecting electrically the impurity diffusion layer via the first opening and the upper electrode via the second opening; forming a local interconnection in a range which pass through the first opening and the second opening and contains at least a region where the upper electrode contacts the oxide dielectric film (figs. 4-5), by patterning the metal film, wherein the local interconnection is a blocking layer for preventing a diffusion of a redundant to the oxide dielectric film; and forming a third insulating film 522/524 for covering the local interconnection such will eliminate the short circuit problems, see figs. 1-6, cols. 1-8.

Kawai et al. discloses a method of forming a semiconductor device, which comprises forming an impurity diffusion layer in a substrate; forming a first insulating film covering the substrate; forming a lower electrode 31 of a capacitor on the first insulating film; forming an oxide dielectric film 32 of the capacitor on the lower electrode; forming an upper electrode 33 of the capacitor on the oxide dielectric film; forming a second insulating film 34 for covering the capacitor; forming a first opening which exposes the impurity diffusion layer and a second opening which exposes the upper electrode in the first and second insulating films, by etching a part of the second insulating film and a part of the first insulating film (figs. 2G); forming a metal film (titanium nitride, which is the same as applicant's claimed invention) on the second insulating film via the first opening and the upper electrode via the second opening, forming a local

interconnection covering an entire portion of the upper electrode with an area which is larger than an area where the upper electrode contacts with the oxide dielectric film in a plan view (i.e., at a plane parallel to the drawing figures, i.e., figs. 1F, 2H), wherein the metal is a blocking layer for preventing a diffusion of a redundant to the oxide dielectric film; and carrying out various steps of oxygen annealing after each the etching steps such will improve the oxide dielectric layer, see fig. 1 A-2H.

The further difference between the references as applied above and the instant claim is claim 5. Yamazaki et al. teaches a method for forming a semiconductor device (capacitor), which comprises patterning the oxide dielectric film and the lower electrode, forming an intermediate insulating film for covering the oxide dielectric film and the lower electrode, forming a window, which is employed to define a capacitor region, in the intermediate insulating film by patterning the intermediate insulating film, and forming the upper electrode at least in the window such will reduce the area of the unit cell, therefore, a dense capacitor can be formed.

Therefore, the subject matter as a whole would have been obvious to one having ordinary skill in the art at the time the invention was made to further modify the standard process of Ochiai or Watanabe et al. with the teaching of Zafar (eliminate the short circuit problems) and Kawai et al. (improve the oxide dielectric layer characteristics) and Yamazaki et al. (reduce the area of the unit cell, therefore, a dense capacitor can be formed) because of the desirability to improve the performance of the device.

Response to Arguments

4. Applicant's arguments filed 6/25/2001 have been fully considered but they are not persuasive.

Applicant argues that none of the applied references, singly or in combination, teach or fairly suggest the significant structural arrangements of the applicants' claim invention concerning forming a local interconnection covering an entire portion of the upper electrode with an area which is larger than an area where the upper electrode contacts with the oxide dielectric film in a plan view. The Examiner disagrees because the figures of Mochizuki et al. (i.e., at a plane parallel to the drawing figures, i.e., see figs.17, 19, 20, 21, 22, 23) and Kawai et al. (i.e., at a plane parallel to the drawing figures, i.e., see figs. 1F, 2H) clearly shows this feature.

Conclusion

5. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37

CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jack Chen whose telephone number is (703) 308-5838. The examiner can normally be reached on Monday-Friday from 8:30 am to 5:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Charles Bowers, can be reached on (703)308-2417.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703)308-0956.

Jack Chen

September 10, 2001

Charles Bowers
Supervisory Patent Examiner
Technology Center 2800